A Quasi Output Voltage Regulation Technique for the Zero Inductor-Voltage Converter

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***Abstract*—The demand for internet and computing resources has led to datacenters and servers being one of the fastest growing consumers of power in the world today. While datacenter power architectures have improved over time, the majority of the loss still occurs at the server power supply, and board level voltage regulators. To attempt to improve this, Google has proposed and implemented a 48 volt server architecture that can significantly reduce both the upstream conversion losses, and the distribution losses within the server racks. To fully realize these benefits new technology is needed to convert 48 volts down to the point of load voltage levels. In this paper a regulation technique for the zero inductor-voltage converter is proposed. This modified control scheme allowed the ZIV converter topology to provide a regulated 12V output from 48/60V input range without sacrificing many of the key advantages that allow the ZIV converter to achieve the highest demonstrated power density and efficiency for intermediate bus converter technologies.**

Keywords—DC-DC Converter, Datacenter, Intermediate Bus

I. Introduction

Intermediate Bus Converters have attracted a very large research interest in recent years, particularly for 48V to 12V conversion in next-generation data center applications. This is because for point of load voltages as low as 1V it is extremely difficult to efficiently achieve this conversion in a single-stage solution. Intermediate Bus Converters can be broadly categorized as non-regulated, and regulated topologies. As shown in Figure 1 it is often advantageous to utilize non-regulated topologies if possible, due to the higher power density and efficiency that can be achieved. However, in some applications, voltage regulation may be required or desirable as the POL converter that is connected to the IBC may operate closer to an optimal point, thus increasing overall system efficiency. The Zero Inductor-Voltage converter, typically operated as an unregulated IBC, achieves the highest power density and efficiency yet demonstrated for 48V to 12V conversion [1]. The Two-Phase 12-Switch ZIV converter design achieved a power density of 2.5kW/in^3 along with a full load 12V/70A efficiency of 97.2%. The work proposed in this paper is a control technique for the ZIV converter, allowing for voltage regulation to be achieved, enabling a 40V-60V input voltage range to be regulated to 12V output. The experimental results presented in this paper are based on the ZIV converter topology shown in Figure 2.

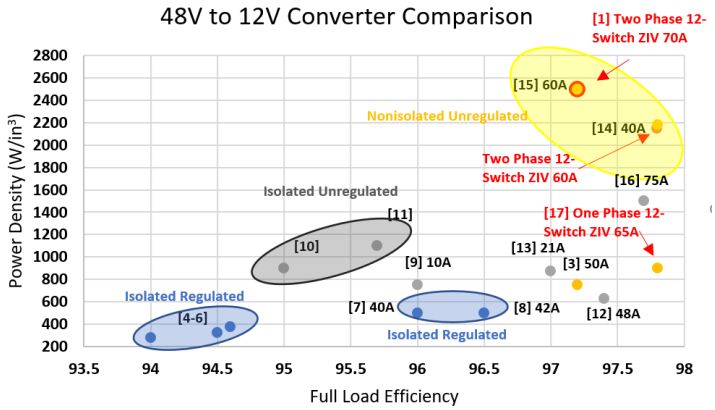

Fig. 1 Comparison of Converter Topologies for 48V to 12V Conversion Referenced From [2]

II. Operating Principles

A. Conventional ZIV Converter Operation

The 7-Switch ZIV converter topology is shown in Figure 2. Under conventional operation this ZIV converter topology achieves an unregulated 4:1 ratio voltage stepdown.

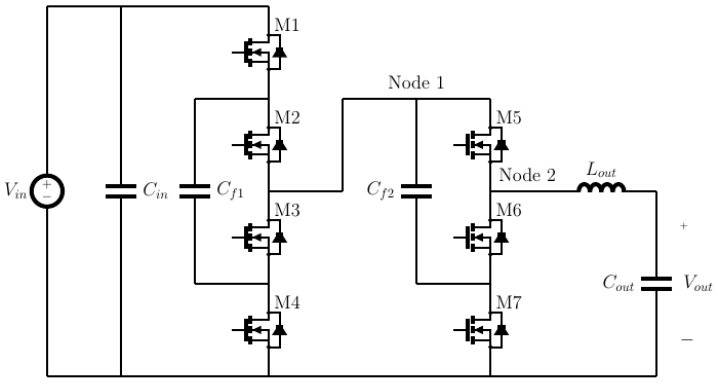

Fig. 2 7-Switch ZIV Converter Topology

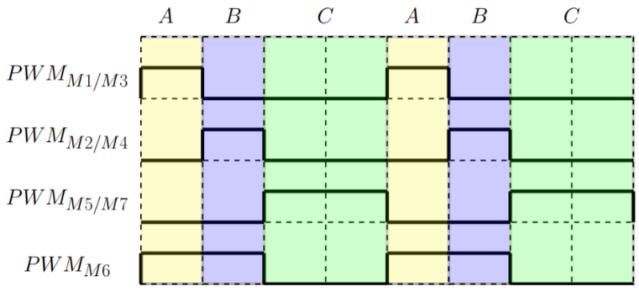

Fig. 3 PWM Gate Diagram for Conventional 7-Switch ZIV Converter Topology

In State A, pictured in Figure 4, MOSFET's M1, M3 and M6 are turned on. Both flying capacitors are charged by the input source.

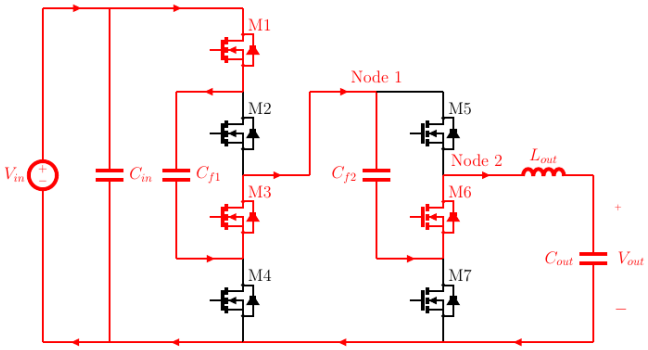

Fig. 4 Circuit State A: Active Components Highlighted in Red

In State A the inductor voltage can be expressed as:

$$V_{LA} = V_{in} - V_{cf1-A} - V_{cf2-A} - V_{out} \quad (1)$$

In State B, shown in Figure 5, MOSFET's M2, M4 and M6 are turned on. In this state the first flying capacitor is now discharging, while the second flying capacitor continues to charge.

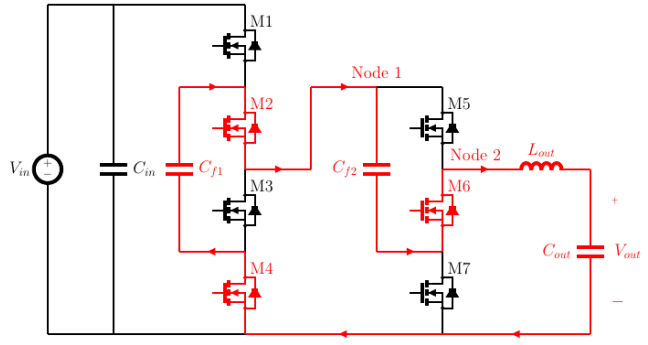

Fig. 5 Circuit State B: Active Components Highlighted in Red

$$V_{LB} = V_{cf1-B} - V_{cf2-B} - V_{out} \quad (2)$$

In State C, illustrated in Figure 6, MOSFET's M5 and M7 are turned on. In this state the first flying capacitor is no longer connected and the second flying capacitor is now discharging.

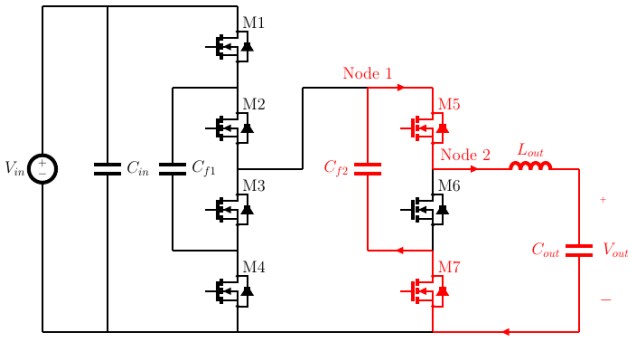

Fig. 6 Circuit State C: Active Components Highlighted in Red

$$V_{LC} = V_{cf2-C} - V_{out} \quad (3)$$

As seen from the gate signal diagram, State A is active for 25% of the switching cycle, State B is active for 25% of the switching cycle, and State C is active for the remaining 50% of the switching cycle. Thus the average inductor voltage can be expressed as:

$$V_L = \frac{V_{LA}}{4} + \frac{V_{LB}}{4} + \frac{V_{LC}}{2} \quad (4.1)$$

$$V_L = \frac{V_{in}}{4} - \left(\frac{V_{cf1-A}}{4} + \frac{V_{cf1-B}}{4}\right) - \left(\frac{V_{cf2-A}}{4} - \frac{V_{cf2-B}}{4}\right) + \frac{V_{cf2-C}}{2} - V_{out} \quad (4.2)$$

Note that the capacitor balance must also be maintained for steady state operation. This means that the average voltage of C_{f1} for State A must be equal to the average voltage of C_{f1} for State B, and the average of C_{f2} across both State A and State B must be equal to the average voltage of C_{f2} across state C. Thus we can simplify the equation by noting the following:

$$V_{cf1-A} = V_{cf2-B} \quad (5)$$

$$\frac{V_{cf2-A} + V_{cf2-B}}{2} = V_{cf2-C} \quad (6)$$

Under steady state operation the average inductor voltage must equal zero over one switching cycle, and as all the capacitor voltage terms cancel out with the above substitutions we are left with:

$$V_{out} = \frac{V_{in}}{4} \quad (7)$$

Thus, the converter achieves 4:1 voltage step down under normal operation. Therefore, in order to achieve voltage regulation, additional operating states must be introduced. These operating states are presented in Figures 7, 8 and 9. In Figure 7, the two low-side MOSFETs (M6 and M7) are turned on, while all other MOSFETs are turned off. In this operating state the on-state MOSFETs operate as synchronous rectifiers, and in this state the output voltage of the converter (at Node 2 before the LC filter) is approximately 0V as the inductor current freewheels through M6 and M7. Therefore, the introduction of this state allows for the average output voltage of the converter to be reduced below 1/4Vin.

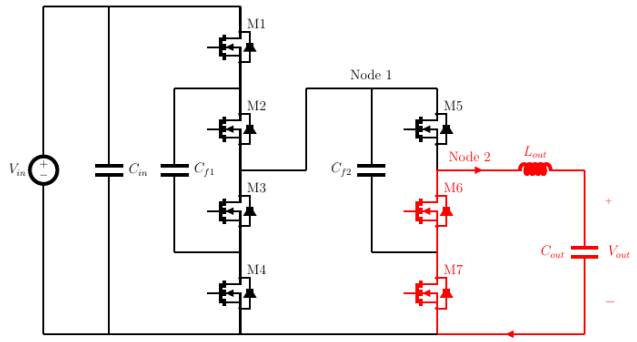

Fig. 7 0V Output "Freewheeling" Operating State

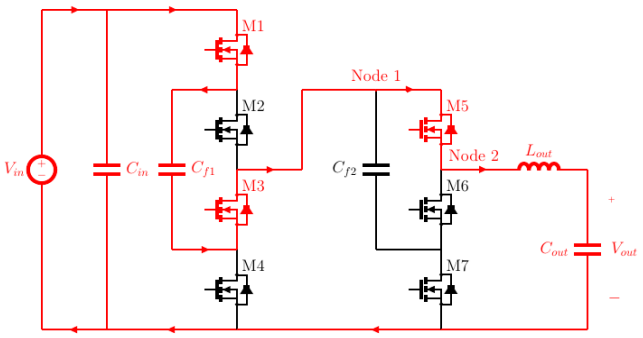

Fig. 8 1/2V_{in} Output "Bypass" Operating State 1

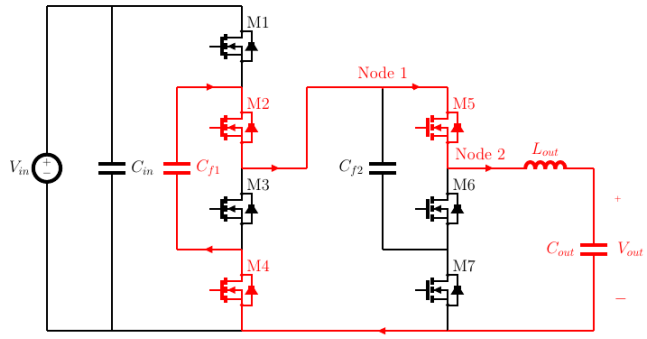

Fig. 9 1/2V_{in} Output "Bypass" Operating State 2

In Figures 8 and 9, the high-side MOSFET (M5) is turned on, while the input stage (M1-M4) continues to operate normally. In this state, the output voltage of the converter (at Node 2 before the LC filter) is approximately 1/2Vin as the second stage is effectively "bypassed". Therefore, the introduction of this state allows for the average output voltage of the converter to be increased above 1/4Vin. Using the combination of these two additional operating states, it is then possible to modify the output voltage of the ZIV converter.

B. Quasi-Regulation Technique

Utilizing the additional operating states presented in Figures 7-9 allows for the output voltage of the ZIV converter to be extended from an unregulated 4:1 stepdown ratio to an arbitrary output voltage ratio between 0V and 2:1 stepdown. First consider the case where a higher stepdown ratio than 4:1 is desired, a common example of this in a practical case would be converting 60V input to 12V output. This can be achieved by utilizing the addition of the "freewheeling" operating state in Figure 7. Note that while the freewheeling operating state can be achieved by turning all the MOSFETs off, this will cause high losses due to the reverse conduction of the body diodes of MOSFETs M6 and M7. Therefore in the practical design it is desirable to turn on M6 and M7 during the freewheeling operating state to prevent the reverse conduction through the body diodes.

The modified output voltage ratio can be understood by examining the output voltage at Node 2 in each switching state. As shown in Section II-A the average of State A, B and C will be equal to a 4:1 stepdown, or 15V for 60V input. It is also clear that the output voltage during the freewheeling state will be equal to approximately 0V, neglecting the voltage drop across the MOSFETs. For the 60V input case the Node 2 voltage will then be a square wave with some average value below 15V depending on the length of the freewheeling state. In the extreme case this voltage can be as low as 0V, with 100% freewheeling time, allowing for any arbitrary output voltage between 15V and 0V to be achieved.

The equation for the output voltage of the converter utilizing the freewheeling state can then be given by equation 8 where t_a, t_b and t_c are the times spent in each switching state respectively, and T_{sw} is the switching period:

$$V_{out} = \frac{\frac{V_{in}}{4}(t_a+t_b+t_c)+0t_{free}}{T_{sw}} \quad (8.1)$$

$$V_{out} = \frac{\frac{V_{in}}{4}(t_a + t_b + t_c)}{T_{sw}} \quad (8.2)$$

Note that it is desirable to keep the ratio of t_a, t_b and t_c equal to the conventional operation of the ZIV converter to minimize the inductor current ripple. That is to say, t_a should be equal to t_b and t_c should be equal to t_a+t_b. It is also desirable to insert the freewheeling time in between the switching transitions, as

shown in Figure 10. This increases the effective frequency seen by the output inductor which reduces the inductor current ripple. From equation 8, to achieve 60V to 12V conversion (5:1 stepdown ratio) the sum of t_a, t_b and t_c should then be 80% of the total switching period, with the remaining 20% of the switching period being the freewheeling operating state. There are three switching transitions in the ZIV converter switching cycle, from State A-B, State B-C, and State C-A. One possible implementation of the freewheeling current state is shown in Figure 10 where freewheeling time is implemented between transitions B-C and C-A. Utilizing a single freewheeling period of 20% of the switching time would give the same average output voltage, but result in a larger magnitude volt-second product across the output inductor, increasing the current ripple.

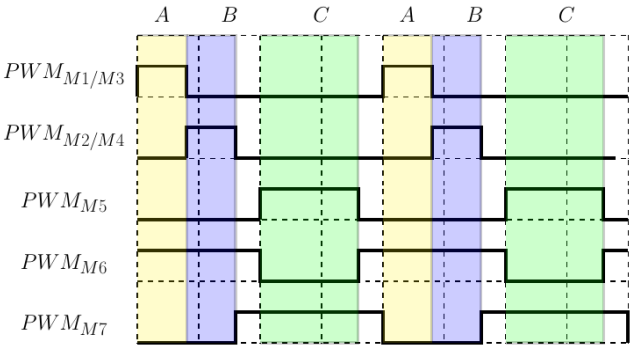

Fig. 10 Example PWM Gate Diagram for Achieving 60V to 12V Conversion with Freewheeling on B-C and C-A Switching Transitions

Adding the freewheeling time on each of the switching transitions would also be possible, but increases the complexity of the PWM signals that need to be generated, which may not be desirable, as the reduction in inductor current ripple as compared with the scheme in Figure 10 is not that drastic. An example of this is shown in Figure 11. Note the additional pulse required on the M7 PWM as compared with Figure 10.

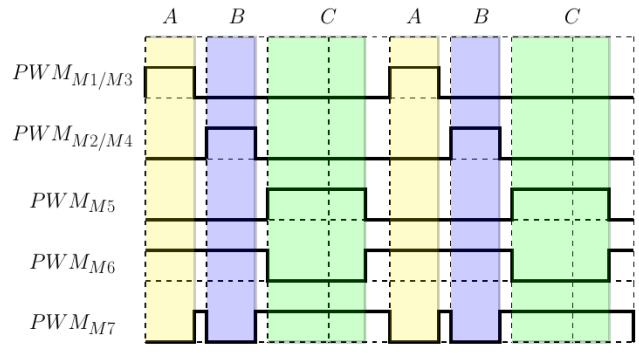

Fig. 11 Example PWM Gate Diagram for Achieving 60V to 12V Conversion with Freewheeling on Every Switching Transition

Similarly, by utilizing the "bypass" operating states shown in Figures 8 and 9 it is possible to increase the output voltage above the nominal 4:1 stepdown ratio. An example of a practical situation where this might be desirable is achieving 12V output from 40V input.

This operation is very similar to the freewheeling operation previously discussed, with the average of State A, B and C again being equal to a 4:1 stepdown ratio, but in this case the bypass operating states output a 2:1 stepdown ratio, rather than 0V. For the 40V input case the Node 2 voltage will then be a square wave with an average value above 10V depending on the length of the bypass states. In the extreme case the voltage can be as high as 20V for 100% bypass time, allowing for any arbitrary voltage between 10V and 20V to be achieved.

The equation for the output voltage of the converter utilizing the freewheeling state can then be given by equation 9 where t_a, t_b and t_c are the times spent in each switching state respectively, t_{bypass} is the time spent in the bypass operating state, and T_{sw} is the switching period:

$$V_{out} = \frac{\frac{V_{in}}{4}(t_a+t_b+t_c)+\frac{V_{in}}{2}t_{bypass}}{T_{sw}} \quad (9)$$

Note that once again it is desirable to keep the ratio of t_a, t_b and t_c equal to that of the conventional ZIV converter. From Equation 9 for 40V to 12V conversion the sum of t_a, t_b and t_c should be 80% of the switching cycle, with he remaining 20% of the switching cycle in the bypass operating states. Furthermore, as shown in Figures 8 and 9, two bypass states are possible. In order to minimize driving circuit complexity, as well as inductor current ripple, it is desirable to implement the bypass operating states on the State B-C and C-A transitions. An example of the PWM gate diagram that could be used to achieve this is presented in Figure 12. It is possible to implement a single bypass operating state for 20% of the switching cycle but this would result in increased volt-second across the inductor, increasing the output current ripple.

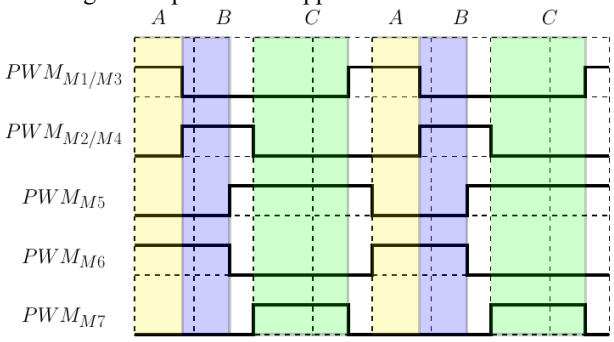

Fig. 12 Example PWM Gate Diagram for Achieving 40V to 12V Conversion With Bypass on B-C and C-A Switching Transitions

The introduction of the freewheeling and bypass operating states increases the ripple current of the output inductor, as the

"zero inductor-voltage" property of the ZIV converter is lost. Therefore, when regulation is required, a larger inductor value is required than would be used for an unregulated ZIV converter. This means that, as with existing topologies, there will be some penalty when regulation of the IBC is required. However, due to the excellent performance of the ZIV converter topology, despite the introduction of this larger inductor, the converter still offers excellent performance in terms of efficiency and power density.

C. *Inductor Sizing*

While the proposed control technique allows the output voltage range of the ZIV converter to be extended, this technique does come at a cost. Compared with a conventional buck converter, the ZIV converter operating at an unregulated 4:1 output mode can utilize a much smaller inductor, as the inductor voltage becomes only the capacitor ripple voltage, and the multilevel structure allows for much lower voltage rated MOSFETs to be utilized. The introduction of the bypass and freewheeling operating states cause the output inductor to see either $1/2V_{in}$ or 0V respectively during these two operating states. Therefore, the inductor size requirement to limit the inductor ripple current increases with the regulation range required. An example of this is presented in the Experimental Results section to follow. For an unregulated, 4:1 ZIV converter achieving 48V to 12V conversion it would be possible to use an inductor as small as 200nH with 60kHz switching [1]. To extend this converter operation to a 60V to 12V conversion, achieving 5:1 stepdown ratio, a 1.8µH inductor with 80kHz switching frequency was used. However, this limitation can be seen in all the topologies presented in Figure 1. By requiring regulation, or quasi-regulation, a penalty in terms of power density and/or efficiency must be paid. It should also be noted that the inductor required will still be much smaller than in a topology like a conventional buck converter. In the buck converter, the inductor voltage will be equal to either V_{in}-V_{out} or -V_{out}. In the case of 60V to 12V conversion this means the buck converter inductor will see approximately 48V for 20% of the switching cycle and -12V for 80% of the switching cycle. In the ZIV converter, achieving the same output voltage ratio, the inductor will see -12V for a total of 20% of the switching cycle, and for the remaining 80% of the switching cycle will see approximately the capacitor ripple voltage. Additionally, as shown in Figure 11, the freewheeling operating states can be introduced in between the switching transitions, increasing the effective frequency seen by the inductor. Therefore the overall volt-second of the inductor will still be substantially reduced compared with a conventional buck converter topology allowing for either a small inductor, or lower switching frequency to be utilized to improve power density and efficiency over conventional topologies.

III. SIMULATION RESULTS

To validate the proposed control technique's ability to modify the output voltage of the ZIV converter, computer simulation is utilized. For both the 60V to 12V and 40V to 12V simulations, the relevant parameters are outlined in Table 1.

Table 1 Simulation Parameters

	Simulation Parameters
Input Voltage	40V-60V
Output Voltage	12V
Output Current	25A
Switching Frequency	100kHz
Flying Capacitor 1	50µF
Flying Capacitor 2	100µF
Inductor	1µH

First the results for the converter operating at 60V to 12V conversion are presented, with a PWM scheme matching that shown in Figure 10. Figure 13 shows the Node 1 voltage for the ZIV converter. This voltage waveform demonstrates that the operation of the first stage is unchanged; the output at Node 1 is equal to $1/2V_{in}$ (30V) during state A and B, and the node is floating during the other operating states. Figure 14 shows the converter output voltage of 12V for 60V input.

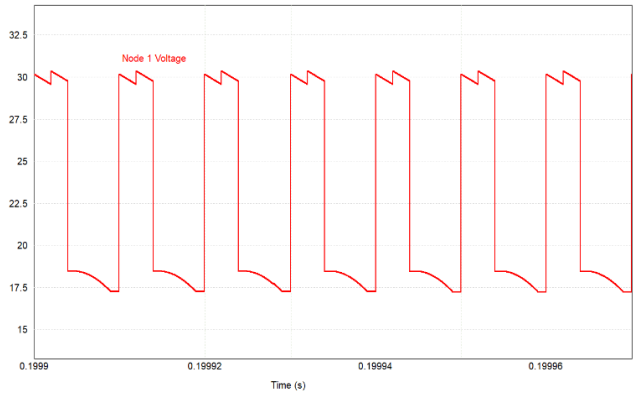

Fig. 13 Node 1 Voltage for 60V to 12V Operation

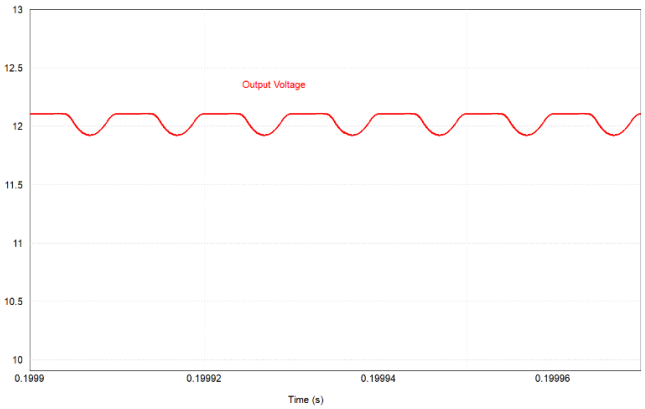

Fig. 14 Output Voltage for 60V to 12V Operation

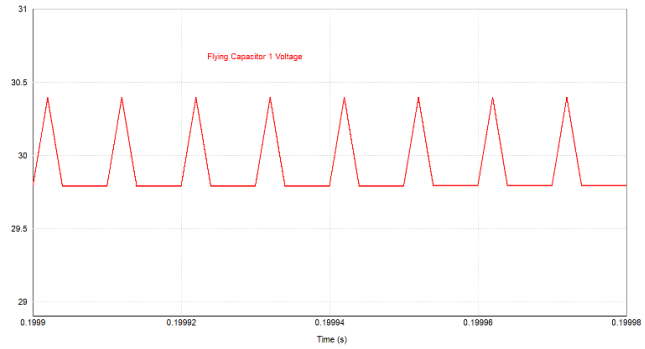

Fig. 15 Flying Capacitor 1 Voltage for 60V to 12V Operation

Figure 15 shows the voltage of the first stage flying capacitor for 60V to 12V operation. As expected the introduction of the freewheeling state does not affect the voltage of this capacitor. Figure 16 shows the voltage of the second stage flying capacitor. Notably, for this capacitor, under normal 4:1 operation the voltage will balance at $1/4V_{in}$. However, with the introduction of the freewheeling state the output voltage will be equal to $1/5V_{in}$ or 12V, instead of 15V. From Equations (7) and (9) this holds true regardless of the voltage of the second stage flying capacitor. As the output from Node 1 is 30V, and the output voltage is 12V, the second stage flying capacitor will be charged to 18V instead of 15V.

$$V_{c2} = V_{node1} - V_{out} \tag{10}$$

This does result in a modest increase in the voltage stress of the MOSFETs, and must be considered in the design.

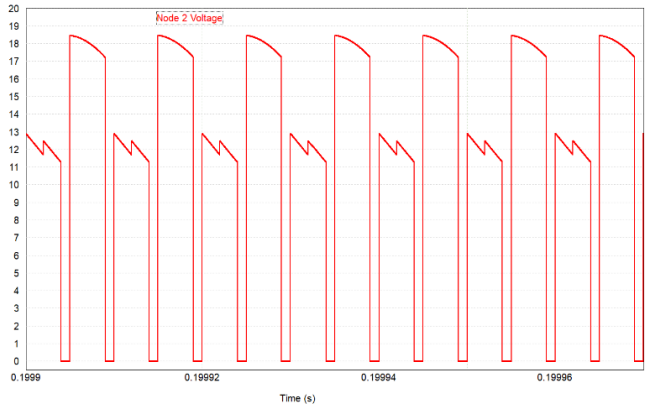

Fig. 16 Node 2 Voltage for 60V to 12V Operation

Figure 17 shows the second stage flying capacitor voltage for 60V to 12V operation of the converter. Note that no capacitor balancing technique is used in either the simulation or the experimental results, thus as with other ZIV converter topologies this operating mode results in self-balancing flying capacitors. A derivation of this is presented in [16].

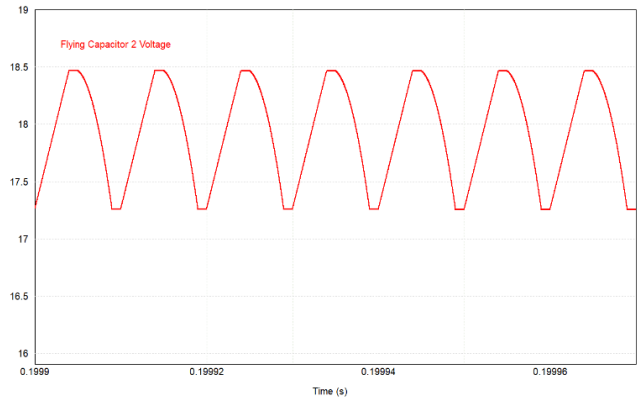

Fig. 17 Flying Capacitor 2 Voltage for 60V to 12V Operation

Results for the 40V to 12V conversion utilizing the bypass operating states are also presented, following the PWM scheme in Figure 12. Figure 18 shows the Node 1 voltage, note that as the input is now 40V the output during State A and B is 20V ($1/2V_{in}$). Figure 19 shows the output voltage of the converter. Figure 20 shows the first stage flying capacitor voltage, which has a nominal value of 20V. Figure 21 shows the node 2 voltage. During the bypass operating states this node is raised to $1/2V_{in}$ or 20V allowing the higher output voltage to be achieved.

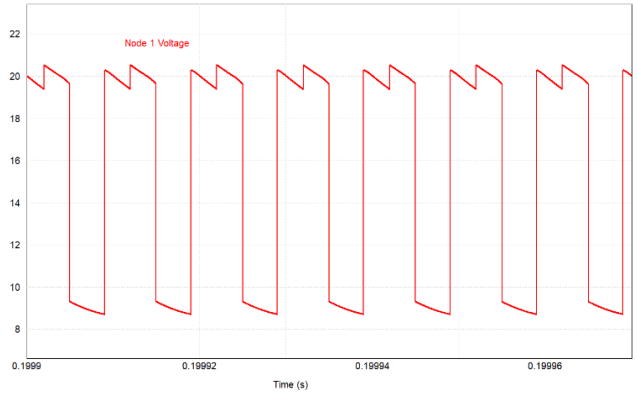

Fig. 18 Node 1 Voltage for 40V to 12V Operation

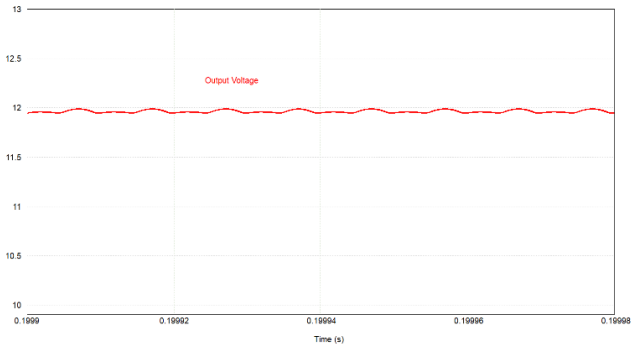

Fig. 19 Output Voltage for 40V to 12V Operation

Figure 22 shows the second stage flying capacitor voltage. As predicted by Equation 10 this capacitor now balances to 8V instead of the nominal 10V for 4:1 stepdown, which must be considered in the design of the MOSFET voltage stress.

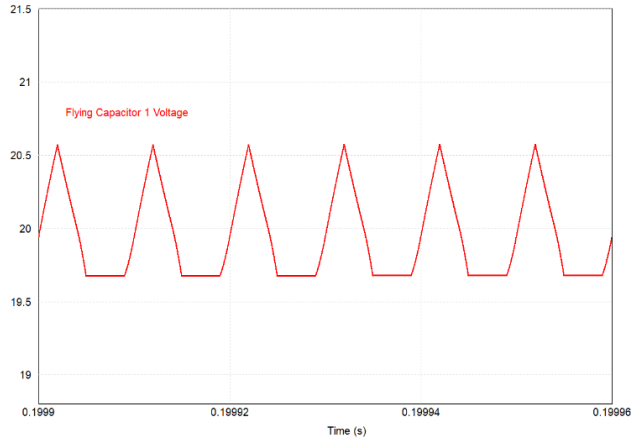

Fig. 20 Flying Capacitor 1 Voltage for 40V to 12V Operation

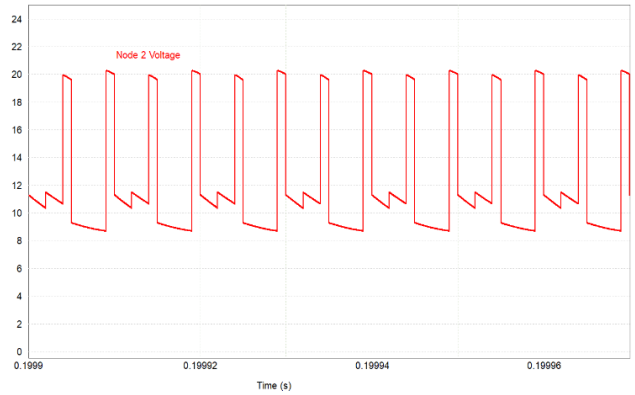

Fig. 21 Node 2 Voltage for 40V to 12V Operation

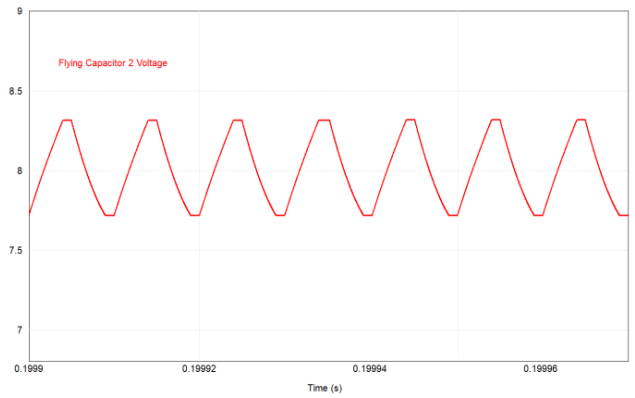

Fig. 22 Flying Capacitor 2 Voltage for 40V to 12V Operation

IV. Experimental Results

A ZIV converter prototype utilizing the components outlined in Table 2 was tested to achieve 48V to 12V conversion, as well as 60V to 12V conversion to validate the proposed ability of the ZIV converter topology to achieve a modified output voltage conversion ratio.

Table 2 Experimental Prototype Components

	Experimental Prototype Components	
	Part Number	***Important Parameters***
M1-M4	BSC011N03LSI	R_{ds}=1.1mΩ Q_g=20nC
M5-M7	BSC009NE2LS5I	R_{ds}=0.95mΩ Q_g=17nC
Inductor	XAL1580-182	L=1.8µH DCR=1.61mΩ
Capacitor 1	10x10µF Ceramic	ESR=1.5mΩ
Capacitor 2	10x47uF Ceramic	ESR=0.75mΩ
Input Capacitor	10x10µF Ceramic	ESR=1.5mΩ

A switching frequency of 80kHz was utilized. The Node 2 voltage waveform for 60V to 12V conversion is shown in Figure 23, demonstrating excellent agreement with the simulated waveforms. The measured prototype efficiency is shown in Figure 24, with a full load efficiency for both 48V to 12V and 60V to 12V at 35A load of more than 97%.

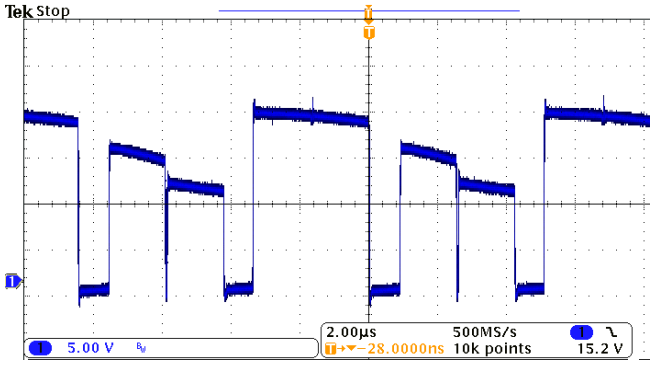

Fig. 23 Node 2 Voltage of Experimental Prototype for 60V to 12V Conversion at 25A Load Current

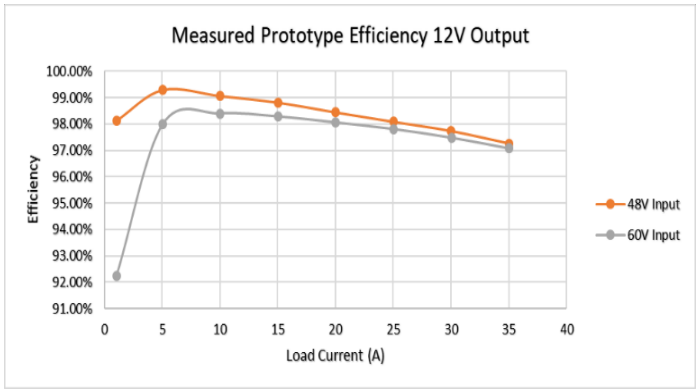

Fig. 24 Experimental Prototype Measured Efficiency

V. Conclusions

The ZIV Converter presented achieves extremely high efficiency for both 48V to 12V and 60V to 12V conversion, with a full load efficiency above 97% and a peak efficiency

above 99%. The measured voltage waveform closely matches the expected simulation and analysis results. Unfortunately, the COVID-19 Pandemic resulted in the closure of the Queen's University laboratory, meaning that further experimental resting including more detailed waveforms as well as verification of the 40V to 12V bypass operating states were not able to be obtained. For the future work this bypass operating state will be tested and validated. Additionally, the proposed voltage output modification technique will be applied to the improved 12-Switch ZIV converter topology, shown in Figure 25.

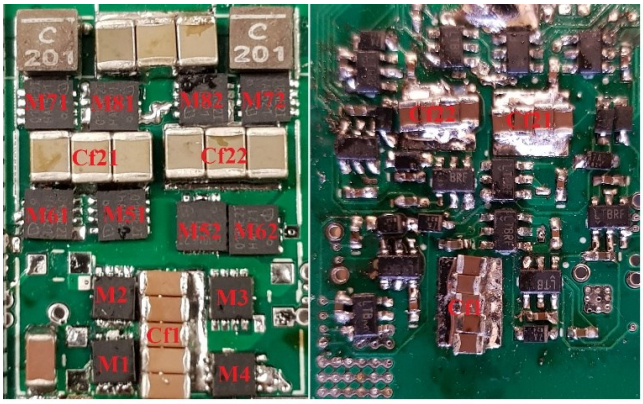

Fig. 25 12-Switch ZIV Converter Topology Achieving 2.5kW/in^3 Power Density for 48V to 12V Conversion as Shown in Figure 1

This topology has demonstrated the highest power density and efficiency in literature for 48V to 12V unregulated conversion [11] and it is expected that with the larger inductor required to achieve quasi-regulation the converter width will increase from 0.75" to 1.1". In this case the power density will still be above 1.6kW/in^3 making this ZIV converter by far the highest power density option where some voltage regulation is required, more than double that of existing regulated IBC solutions.

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